Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.100”**

**.075”**

**GATE**

**.018 X .025”**

**SOURCE**

**.018 X .025”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .018” X .025”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .075” X .100” DATE: 2/24/17**

**MFG: INT’L RECTIFIER THICKNESS .019” P/N: IRFC310N**

**DG 10.1.2**

#### Rev B, 7/1